

What is claimed:

- 1 1. A semiconductor device comprising:  
2 a pad section over an interlayer dielectric layer,  
3 wherein the interlayer dielectric layer includes a first silicon oxide layer that is  
4 formed by a polycondensation reaction of a silicon compound and hydrogen peroxide, and a  
5 second silicon oxide layer formed over the first silicon oxide layer and containing an  
6 impurity, and  
7 the pad section includes a wetting layer and a metal wiring layer.
- 1 2. A semiconductor device according to claim 1, wherein the impurity contained  
2 in the second silicon oxide layer is phosphorous.
- 1 3. A semiconductor device according to claim 1, wherein the metal wiring layer  
2 is formed from aluminum or an aluminum alloy.
- 1 4. A semiconductor device according to claim 1, wherein the wetting layer is  
2 formed from a material that is selected from titanium, cobalt, zirconium, silicon and  
3 niobium.
- 1 5. A semiconductor device according to claim 1, wherein the metal wiring layer  
2 includes an alloy layer that contacts the wetting layer, the alloy layer including a material  
3 that forms the wetting layer and a material that forms the metal wiring layer.
- 1 6. A semiconductor device according to claim 5, wherein the alloy layer has a  
2 film thickness that is two to three times greater than a film thickness of the wetting layer.
- 1 7. A semiconductor device according to claim 1, wherein the pad section does  
2 not have a nitride layer.

- 1     8.     A method for manufacturing a semiconductor device, comprising the steps  
2 of:  
3     (a) forming a interlayer dielectric layer, the step including:  
4         (a) (1) forming a first silicon oxide layer by reacting a silicon compound and  
5             hydrogen peroxide through a chemical vapor deposition method, and  
6         (a) (2) forming a second porous silicon oxide layer by reacting a silicon  
7             compound, at least one of oxygen and a compound including oxygen, and a  
8             compound including an impurity through a chemical vapor deposition  
9             method;  
10        (b) forming a wetting layer over the interlayer dielectric layer;  
11        (c) forming a metal wiring layer over the wetting layer; and  
12        (d) forming a pad section by patterning the wetting layer and the metal wiring layer.

- 1     9.     A method for manufacturing a semiconductor device according to claim 8,  
2 further comprising, after the step (a), the step of conducting an anneal treatment at a  
3 temperature of 600 – 850°C.

- 1     10.    A method for manufacturing a semiconductor device according to claim 8,  
2 wherein the silicon compound used in the step (a) (1) is at least one type selected from an  
3 inorganic silane compound including monosilane, disilane,  $\text{SiH}_2\text{Cl}_2$  and  $\text{SiF}_4$ , or an organo  
4 silane compound including  $\text{CH}_3\text{SiH}_3$ , tripropyl-silane and tetraethylorthosilicate.

- 1     11.    A method for manufacturing a semiconductor device according to claim 8,  
2 wherein the step (a) (1) is conducted with the silicon compound being an inorganic silane  
3 compound by a reduced pressure chemical vapor deposition method at a temperature of 0 –  
4 20°C.

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1 12. A method for manufacturing a semiconductor device according to claim 8,  
2 wherein the step (a) (1) is conducted with the silicon compound being an organo silane  
3 compound by a reduced pressure chemical vapor deposition method at a temperature of 100  
4 - 150°C.

1 13. A method for manufacturing a semiconductor device according to claim 8,  
2 wherein the step (a) (2) is conducted by a plasma chemical vapor deposition method at a  
3 temperature of 300 - 450°C.

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1 ~~14~~. A method for manufacturing a semiconductor device according to claim ~~13~~,  
2 wherein the compound including oxygen used in the step (a) (2) is dinitrogen monoxide.

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1 15. A method for manufacturing a semiconductor device according to claim 8,  
2 wherein the step (a) (2) is conducted by a chemical vapor deposition method at a  
3 temperature of 300 - 550°C.

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1 ~~16~~. A method for manufacturing a semiconductor device according to claim ~~15~~,  
2 wherein the compound including oxygen used in the step (a) (2) is ozone.

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1 17. A method for manufacturing a semiconductor device according to claim 8,  
2 wherein, before forming the second silicon oxide layer in the step (a) (2), the first silicon  
3 oxide layer is exposed to an ozone atmosphere.

1 18. A method for manufacturing a semiconductor device according to claim 8,  
2 wherein the impurity used in the step (a) (2) is phosphorous.

1 19. A method for manufacturing a semiconductor device according to claim 8,  
2 wherein the metal wiring layer is provided by forming a first aluminum layer including  
3 aluminum or an alloy containing aluminum as a main component at a temperature of 200°C  
4 or lower, then forming a second aluminum layer including aluminum or an alloy containing  
5 aluminum as a main component at a temperature of 300°C or higher.

1 20. A method for manufacturing a semiconductor device, comprising:  
2 forming a first silicon oxide layer using a polycondensation reaction of a silicon  
3 compound and hydrogen peroxide;  
4 forming a second silicon oxide layer including an impurity therein; and  
5 forming a pad section over the first silicon oxide layer and the second silicon oxide  
6 layer, the pad section including a wetting layer and a wiring layer.

1 21. A method as in claim 20, comprising forming the second silicon oxide layer  
2 to be more porous than the first silicon oxide layer.